

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	
		Filing Date	
		First Named Inventor	Buchty et al.
		Art Unit	
		Examiner Name	
Sheet 1 of 1	Attorney Docket Number	Buchty 1-7-1	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
st		R. ESPASA, M. VALERO, J. SMITH, Vector Architectures: Past, Present and Future, International Conference on Supercomputing (ICS'1998), pp. 425-432, July 1998	
st		Pages downloaded from home.ecn.ab.ca/~jsavard/other/arcint.htm,ar02.htm,ar0201.htm,ar0202.htm,ar020201.htm,ar0302htm,ar0304.htm; downloaded on 11/24/03	
st		P. KOOPMAN, Vector Architecture, Carnegie Mellon 18-548/15-548 Memory System Architecture, 11/4/98, downloaded from www.ece.cmu.edu/~ece548/handouts/16v_arch.pdf on 11/24/03	
st		W. BUCHHOLZ, The IBM System/370 vector architecture, IBM Systems Journal, Vol. 25, No. 1, 1986, pp. 51-62	
st		M. MITTAL, A. PELEG, U. WEISER, MMX Technology Architecture Overview, Intel Technology Journal, 3rd Quarter 1997, www.intel.com/technology/itj/q31997/pdf/archite.pdf	
st		A. PELEG, U. WEISER, MMX Technology Extension to the Intel Architecture, IEEE Micro, 1996, pp. 42-50	
st		Motorola, AltiVec Technology At-a-Glance, 2002, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECGLANCE.pdf	
st		S. FULLER, Motorola's AltiVec Technology, 1998, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECWP.pdf	
st		Motorola, AltiVec Execution Unit and Instruction Set Overview, downloaded from http://e-www.motorola.com/webapp/sps/site/overview.jsp?nodeId=03C1TR0467mKqW5Nf2hG12 11/24/03	
st		V. FISCHER, M. DRUTAROVSKY, Scalable RSA Processor in Reconfigurable Hardware - a SoC Building Block, Conf. on Design of Circuits and Integrated Sys., 11/ 20-23/01, Portugal	

Examiner Signature	<i>Sheng-Jin Jia</i>	Date Considered	3/29/2006
--------------------	----------------------	-----------------	-----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.